I CLAIM

1. A method of simulating operation of data processing apparatus including a plurality of pipelined circuit elements driven by a common clock signal, said method using a plurality of pipelined circuit element models linked by one deep message queues and a set of data storage areas and comprising the steps of:

(i) within a first data storage area storing input data values representing respective input signals passed to each pipelined circuit element at commencement of a simulated common clock signal cycle of said common clock signal;

(ii) during simulation of said simulated common clock signal cycle reading said input data values for each pipelined circuit element from said first data storage area and using a pipelined circuit element model for each pipelined circuit element to generate output data values representing output signals generated by said pipelined circuit element by termination of said simulated common clock signal cycle;

(iii) within a second data storage area storing said output data values; and

(iv) changing said second data storage area to serve as said first data storage area such that said stored output data values may serve as input data values during a following simulated clock signal cycle and changing to use a different storage area as said second storage area.

2. A method as claimed in claim 1, wherein said first data storage area and said second data storage area swap roles such that newly generated output data values may overwrite input data values for a preceding simulated common clock signal cycle.

3. A method as claimed in claim 1, wherein at least some of said input data values and said output data values represent signal values passed via latches between adjacent serially arranged pipelined circuit elements.

4. A method as claimed in claim 1, wherein at least some of said output data values represent signal values received from non-pipelined circuit elements.

5. A method as claimed in claim 4, wherein at least some of said input data values represent signal values passed to said non-pipelined circuit elements.

6. A method as claimed in claim 5, wherein any output data values from a non-pipelined circuit element model are generated after generation of and using any output data values produced elsewhere that serve as input data values to said non-pipelined circuit element model.

7. A method as claimed in claims 4, wherein at least one of said non-pipelined circuit elements is passed non-latched input data values directly from one or more of said pipelined circuit element models.

8. A method as claimed in claim 1, wherein said pipeline circuit element models are software models that map input data values to output data values.

9. A method as claimed in claim 1, wherein said data processing apparatus includes multiple clock domains, each clock domain being associated with a separate plurality of pipelined circuit elements, clocking of each plurality of pipelined circuit elements being separately simulated.

10. A method as claimed in claim 1, wherein said data processing apparatus includes a pipelined processor.

11. A method as claimed in claim 10, wherein each processor pipeline stage corresponds to a pipelined circuit element model.

12. A method as claimed in claim 1, wherein said first data storage area corresponds to a first address region within a common memory.

13. A method as claimed in claim 12, wherein said second data storage area corresponds to a second address region within said common memory.

14. A method as claimed in claim 1, wherein said plurality of pipelined circuit element model are subject to compile time scheduling to form a single functional block.

15. Apparatus for simulating operation of data processing apparatus including a plurality of pipelined circuit elements driven by a common clock signal, said apparatus using a plurality of pipelined circuit element models linked by one deep message queues and comprising:

(i) a first data storage area for storing input data values representing respective input signals passed to each pipelined circuit element at commencement of a simulated common clock signal cycle of said common clock signal;

(ii) a pipelined circuit element model for each pipelined circuit element operating during simulation of said simulated common clock signal cycle to read said input data values for each pipelined circuit element from said first data storage area and to use said input data values to generate output data values representing output signals generated by said pipelined circuit element by termination of said simulated common clock signal cycle;

(iii) a second data storage area for storing said output data values; and

(iv) control logic for changing said second data storage area to serve as said first data storage area such that said stored output data values may serve as input data values during a following simulated clock signal cycle and changing to use a different storage area as said second storage area.

16. A computer program storage medium storing a computer program for controlling a computer to perform a method of simulating operation of data processing apparatus including a plurality of pipelined circuit elements driven by a common clock signal, said method using a plurality of pipelined circuit element models linked by one deep message queues and comprising the steps of:

(i) within a first data storage area storing input data values representing respective input signals passed to each pipelined circuit element at commencement of a simulated common clock signal cycle of said common clock signal;

(ii) during simulation of said simulated common clock signal cycle reading said input data values for each pipelined circuit element from said first data storage area and using a pipelined circuit element model for each pipelined circuit element to

generate output data values representing output signals generated by said pipelined circuit element by termination of said simulated common clock signal cycle;

(iii) within a second data storage area storing said output data values; and

(iv) changing said second data storage area to serve as said first data storage area such that said stored output data values may serve as input data values during a following simulated clock signal cycle and changing to use a different storage area as said second storage area.